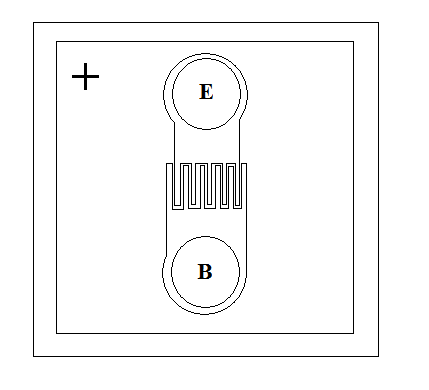
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.014”**

**.014”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” min**

**Backside Potential: Collector**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .014” x .014” DATE: 9/23/21**

**MFG: ST MICRO THICKNESS .008” P/N:BFRC96**

**DG 10.1.2**

#### Rev B, 7/19/02